EXXELIA

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Miniaturization of high voltage MLCC for space applications

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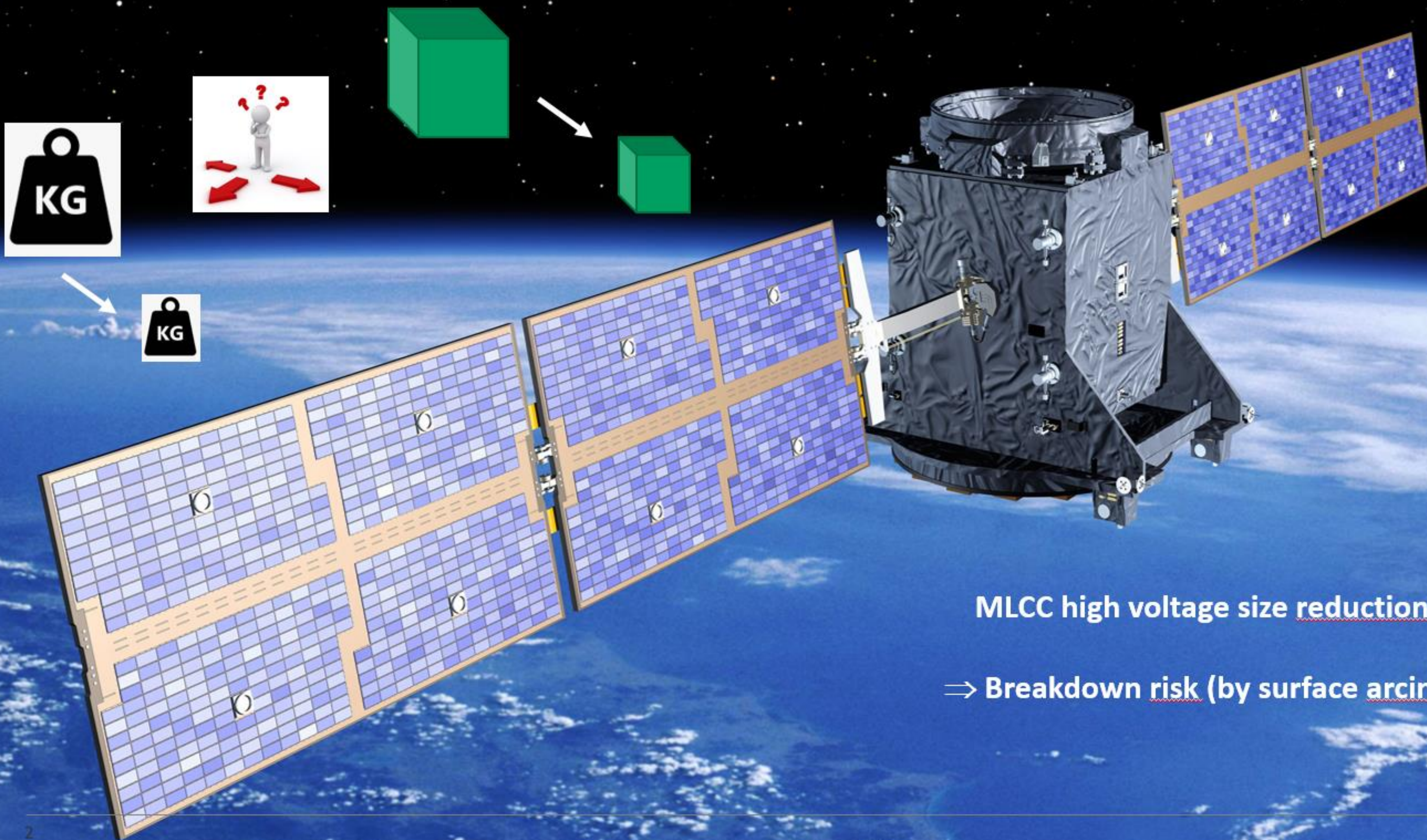
Miniaturization in space field : a permanent challenge



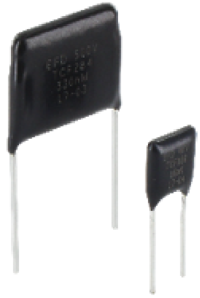
MLCC high voltage size reduction

⇒ Breakdown risk (by surface arcing)

MLCC high voltage space parts reduction :

For single leaded MLCC parts :

- external surface arcing risk is avoided by external varnishing, coating or molding



For stacked MLCC parts :

- external surface arcing risk can be avoided by external potting
- arcing risk remains on the areas between the chips, because of presence of gas

Breakdown voltage in low-pressure gaseous environment

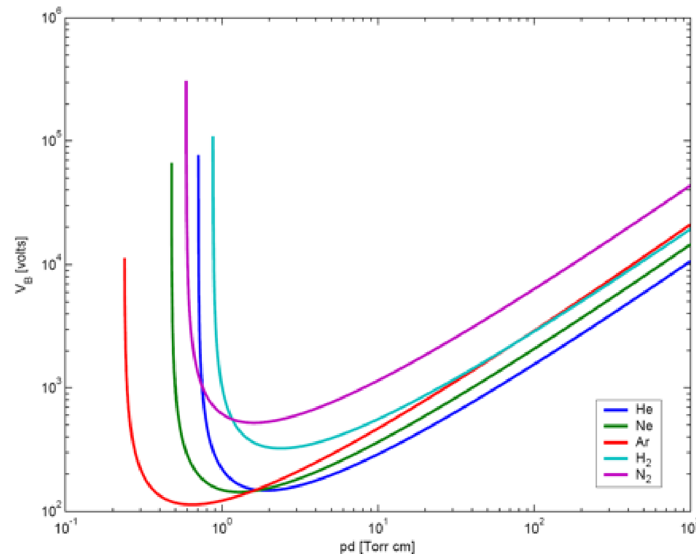
Basic breakdown mechanism is caused by collision of charges in the gas volume and their interactions with the electrode surface (Townsend mechanism) :

- the electric field accelerates free electrons inside gas-filled gap, which collide with gas atoms

- if kinetic energy of these electrons is high enough => gas atoms ionization => new electrons release

- avalanche of electrons can grow towards the anode, while the ions moving in the opposite direction collide with the cathode releasing new electrons

=> a well ionized conductive channel can develop in few µseconds



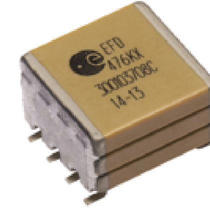
As a consequence of avalanche breakdown, there is always a balance where molecule distance (given by gas pressure) and electric field strength (given by total gap distance) are providing optimum conditions for ionization => very low breakdown voltage.

This physical relation is expressed by the ''Paschen Law'' and corresponding ''Paschen Curve'', which gives a minimum breakdown voltage of 330V.

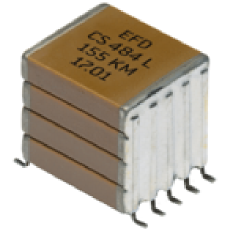
To mitigate this issue, an insulating material is applied on the surface of high voltage components

Exxelia solution for smaller parts

Higher capacitance/same nominal voltage in a smaller footprint => stack of smaller parts



CNC3x CNC5x already existing QPL series => Exxelia manages stacking for space grade, but by now for low voltages (16V to 500V ; 2220 to 8060 size)



CS1xx-CS4xx-CS2xx already existing series => Exxelia manages stacking of standard high voltage (total insulation not mandatory)

For high voltage space applications, Exxelia's solution is an interchip filling material :

- Isolating enough
- Compatible with component finishing steps (leadframes soldering)
- Customer use (mounting)

=> Glass filling material, applied on chips before stacking

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Glass filling material insulation

Filling material is mandatory to increase electrical breakdown strength between opposite poles of the parts but its use has to be controlled.

Glass filling material use for insulation means :

Glass filling material deposition management :

- Deposition tools
- Deposition parameters
- Chips preparation
- Glass thermal treatment

But also effect of glass filling on :

- Parts finishing steps (soldering)
- Electrical behaviour of the stacks (ESR)
- Thermomechanical behaviour of stacks

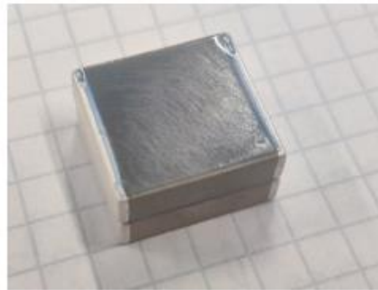
Glass filling management

Previous Exxelia studies => no glass on end terminations (soldering and ESR issues)

- Automatic deposition equipment used

- Deposition trials to optimize the layout after sintering :
    - Quantity
    - On one or both parts to stack
    - Direct sintering or prereflow need
    - Gap to be full-filled or not

Preliminary full–filled tests => glass leakage during sintering (reflow) cycle



=> single glass line insulation

Test vehicles

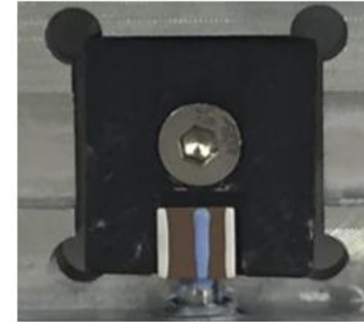
Size and insulation protocole :

2220 parts (small size)

2 parts stacks

Glass deposition protocole :

- Deposition of the glass on one chip
- Glass layout levelling step
- Stacking of the 2nd chip
- Glass drying step
- Glass burn-out and sintering steps



Single line after deposition

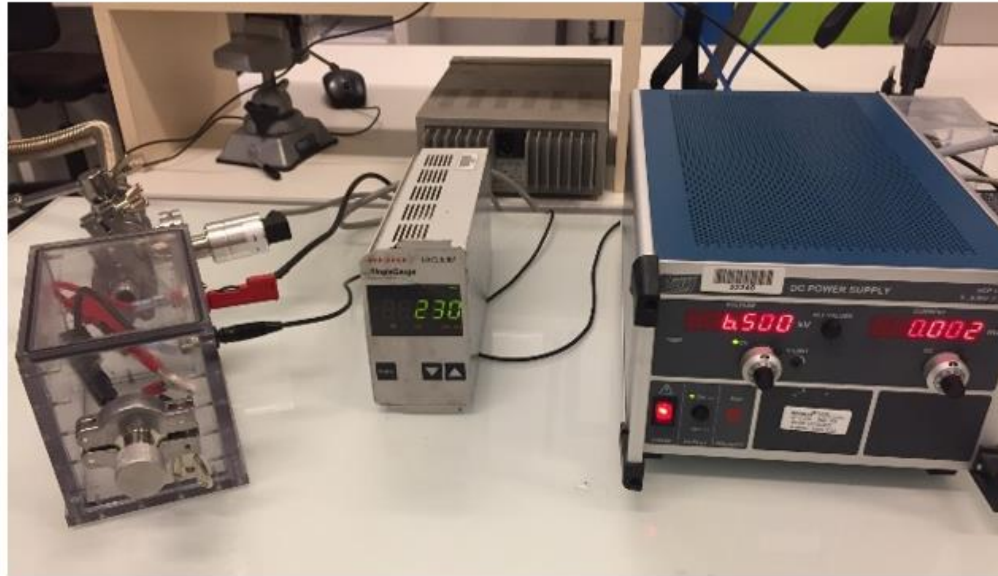
Single line glass insulation
(parallel to end terminations)

Single line after sintering

Electrical behaviour simulation

Why ? To show pressure effect on withstanding voltage values, to validate/invalidate Exxelia HV stacks useability for aeronautics/space applications

How ? On 2220 parts without any internal electrodes (to check external withstanding of the stacks, not internal dielectric withstanding), test of withstanding voltage change between atmospheric pressure and 200-250mbar (equivalent to long flight cruise altitude)

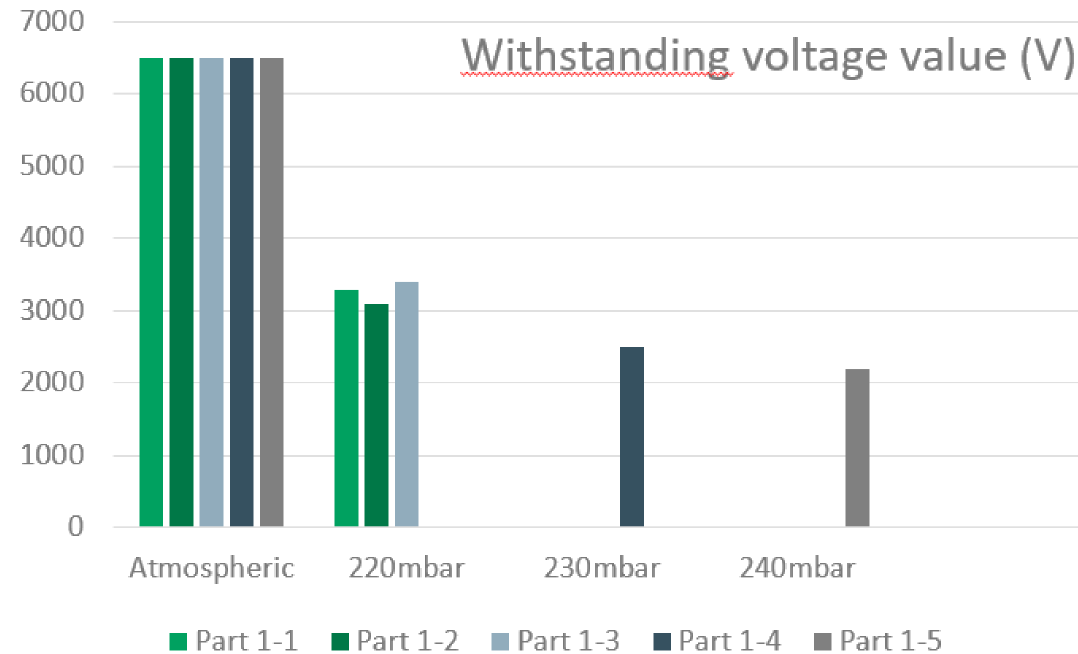


In-house low pressure withstanding measurement equipment
(power supply : 6500V max

Withstanding voltage reference

Withstanding references values generated on :

- 2220 bare (no glass barrier) single parts
- At atmospheric pressure
- Under low pressure (220-240mbar) range



Significant and noticeable decrease of withstanding voltage values at low pressure

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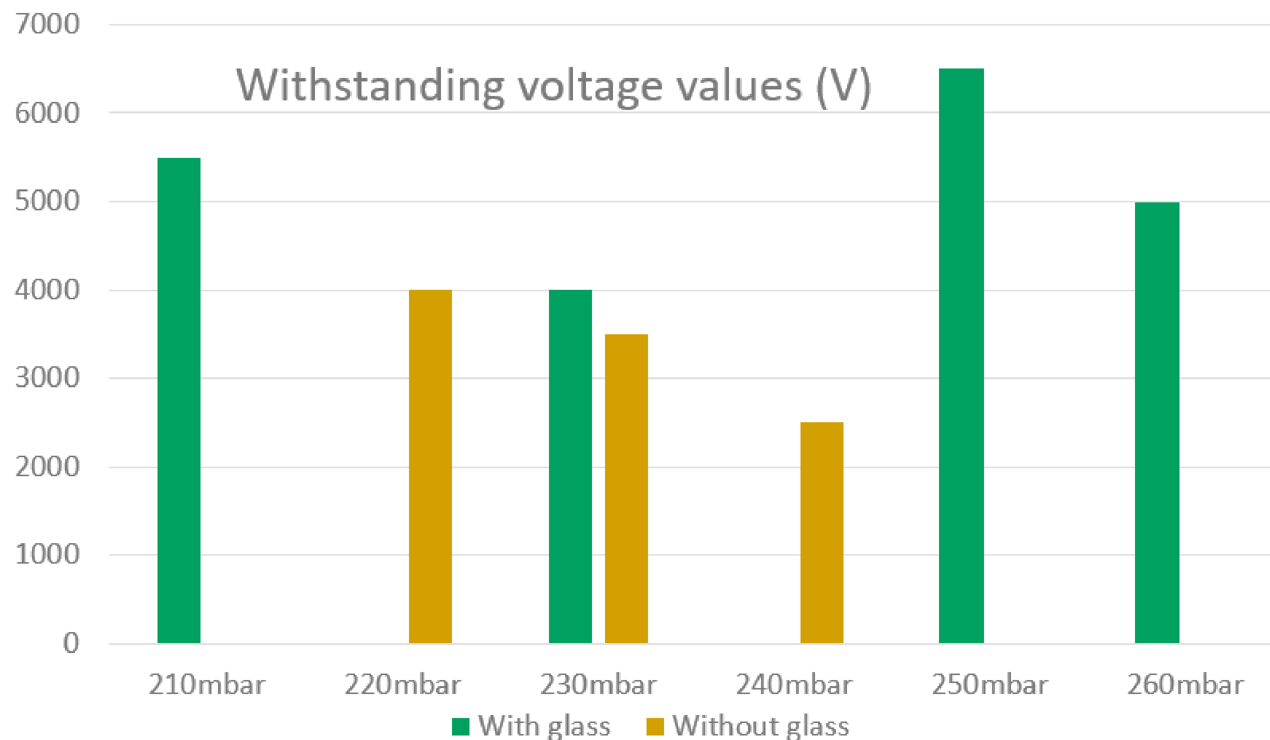
Influence of glass barrier presence on withstanding values

Withstanding values generated on :

- 2220 2 chips stacks (same lot as parts used for reference)
- With single line barrier vs no barrier stacks
- Stacks externally covered with a silicone varnish (customer potting simulation=external leakage prevention)
- Under low pressure (220-240mbar) range



Withstanding voltage values are globally higher with glass barrier

But, because of varnish, no way to check where the breakdown occurs

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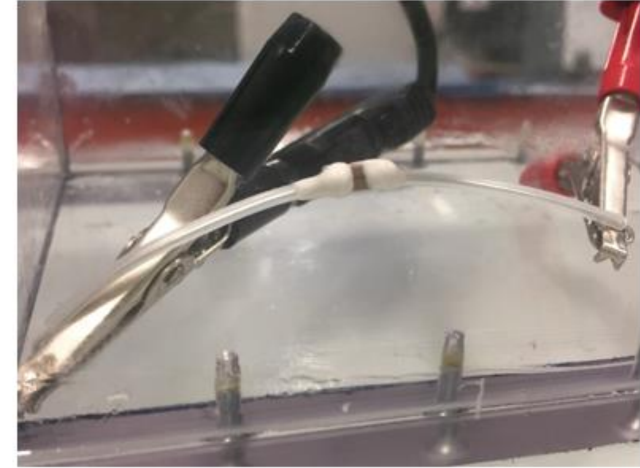
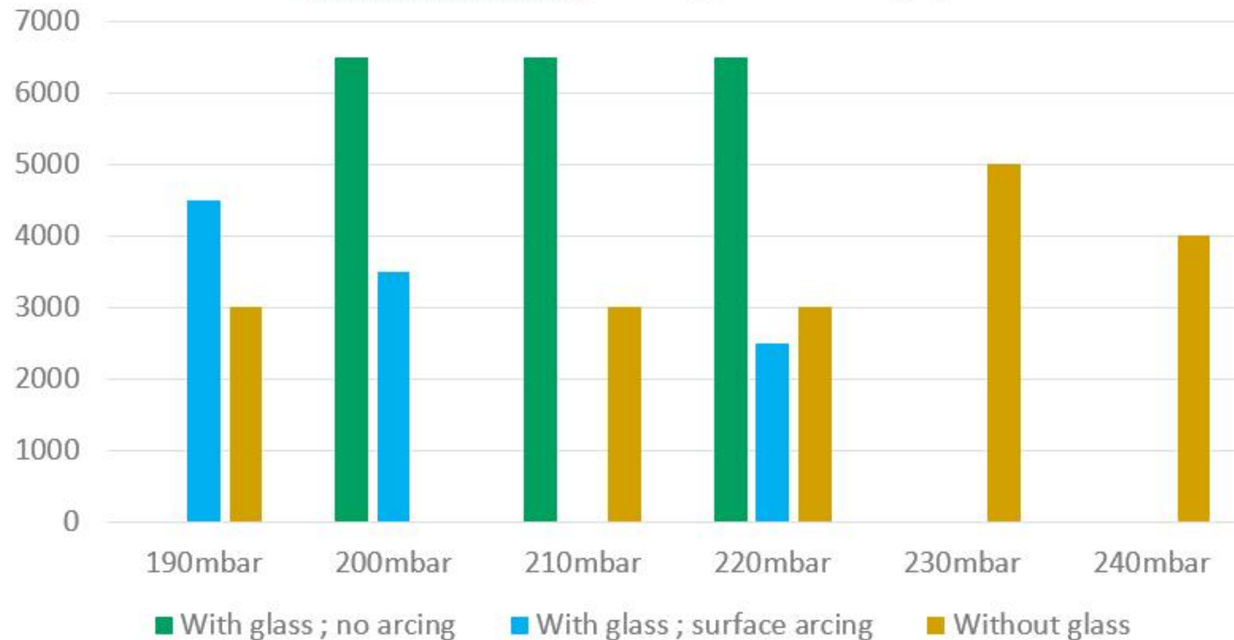
Localization of the electrical leakage

Withstanding values generated on :

- 2220 2 chips stacks (same lot as parts used for reference)
- With single line barrier vs no barrier stacks
- No varnish but end terminations insulation
- Under low (220-240mbar) pressure



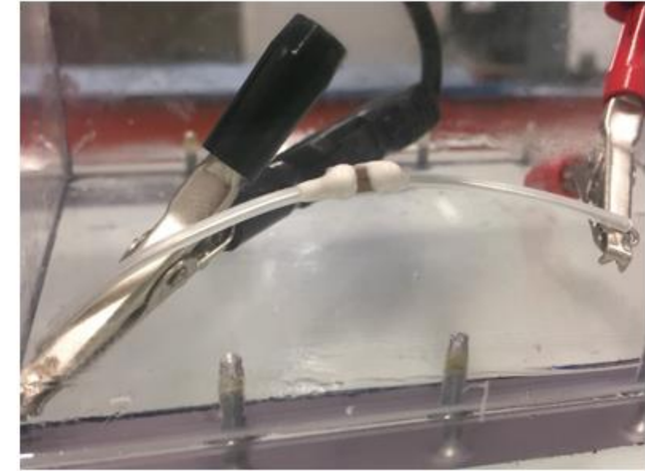


Low pressure withstanding voltage values are similar to the reference ones at atmospheric pressure => **glass barrier is efficient**

Leakage occurred on some parts at the surface of the glass (unvarnished surfaces on the sides of the stacks)

For all stacks without glass, arcing occurs between chips

Localization of the electrical leakage, under very low pressure



Withstanding values generated on :

- 2220 2 chips stacks (same lot as parts used for reference)
- With single line barrier
- No varnish but end terminations insulation
- Under low (220-240mbar) or very low (21mbar) pressure

2 parts 2220 stacks with single line glass barrier :

- 6500V under 210 mbars
- 2000V under 21mbars, but with arcing between voltage supply clamps, not on parts

In very low pressure environment, arcing still occured but not on part

For such low pressure, measurement configuration has to be improved to check the real withstanding value

Conclusion

Exxelia's solution to manufacture reliable HV stacks useable for aeronautics and space conditions seems to work

It's a promising technology to decrease capacitor footprints in space applications

Additional studies are in progress to confirm this technology on various configurations (ceramics, sizes and thicknesses of chips) and also on functionnal HV parts (with electrodes)

Do you have any questions?

Thank you for your attention